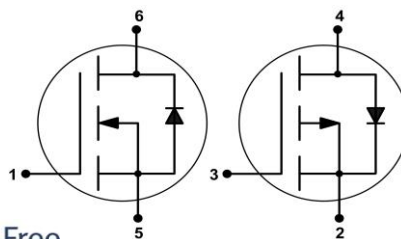
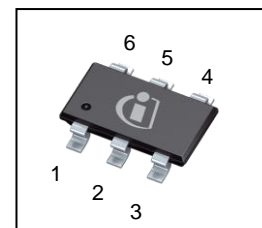


**OptiMOS™ 2 + OptiMOS™-P 2 Small Signal Transistor**
**Features**

- Complementary P + N channel
- Enhancement mode
- Logic level (4.5V rated)
- Avalanche rated
- Qualified according to AEC Q101
- 100% lead-free; RoHS compliant
- Halogen free according to IEC61249-2-21

**Product Summary**

		<b>P</b>	<b>N</b>	
$V_{DS}$		-30	30	V
$R_{DS(on),max}$	$V_{GS}=\pm 10\text{ V}$	150	160	mΩ
	$V_{GS}=\pm 4.5\text{ V}$	270	280	
$I_D$		-1.5	1.4	A


**PG-TSOP6**


Type	Package	Tape and Reel Information	Marking	Lead Free	Packing
BSL316C	PG-TSOP-6	H6327: 3000 pcs / reel	sPJ	Yes	Non dry

**Maximum ratings, at  $T_j=25\text{ °C}$ , unless otherwise specified <sup>1)</sup>**

Parameter	Symbol	Conditions	Value		Unit
			<b>P</b>	<b>N</b>	
Continuous drain current	$I_D$	$T_A=25\text{ °C}$	-1.5	1.4	A
		$T_A=70\text{ °C}$	-1.2	1.1	
Pulsed drain current	$I_{D,pulse}$	$T_A=25\text{ °C}$	-6.0	5.6	
Avalanche energy, single pulse	$E_{AS}$	P: $I_D=-1.5\text{ A}$ , N: $I_D=1.4\text{ A}$ , $R_{GS}=25\text{ }\Omega$	11	3.7	mJ
Gate source voltage	$V_{GS}$		$\pm 20$		V
Power dissipation <sup>1)</sup>	$P_{tot}$	$T_A=25\text{ °C}$	0.5		W
Operating and storage temperature	$T_j, T_{stg}$		-55 ... 150		°C
ESD class		JESD22-A114-HBM	0 (<250V)		
Soldering temperature	$T_{solder}$		260		°C
IEC climatic category; DIN IEC 68-1			55/150/56		

<sup>1)</sup> Remark: only one of both transistors active

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

**Thermal characteristics**

Thermal resistance, junction - ambient <sup>1)</sup>	P	$R_{thJA}$	minimal footprint <sup>2)</sup>	-	-	250	K/W
	N						

**Electrical characteristics, at  $T_j=25\text{ }^\circ\text{C}$ , unless otherwise specified**
**Static characteristics**

Drain-source breakdown voltage	P	$V_{(BR)DSS}$	$V_{GS}=0\text{ V}, I_D=-250\text{ }\mu\text{A}$	-	-	-30	V
	N		$V_{GS}=0\text{ V}, I_D=250\text{ }\mu\text{A}$	30	-	-	
Gate threshold voltage	P	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=-11\text{ }\mu\text{A}$	-2	-1.5	-1	
	N		$V_{DS}=V_{GS}, I_D=3.7\text{ }\mu\text{A}$	1.2	1.6	2	
Zero gate voltage drain current	P	$I_{DSS}$	$V_{DS}=-30\text{ V}, V_{GS}=0\text{ V}, T_j=25\text{ }^\circ\text{C}$	-	-	-1	$\mu\text{A}$
	N		$V_{DS}=30\text{ V}, V_{GS}=0\text{ V}, T_j=25\text{ }^\circ\text{C}$	-	-	1	
	P		$V_{DS}=-30\text{ V}, V_{GS}=0\text{ V}, T_j=150\text{ }^\circ\text{C}$	-	-	-100	
	N		$V_{DS}=30\text{ V}, V_{GS}=0\text{ V}, T_j=150\text{ }^\circ\text{C}$	-	-	100	
Gate-source leakage current	P	$I_{GSS}$	$V_{GS}=\pm 20\text{ V}, V_{DS}=0\text{ V}$	-	-	$\pm 100$	nA
	N						
Drain-source on-state resistance	P	$R_{DS(on)}$	$V_{GS}=-4.5\text{ V}, I_D=-1.1\text{ A}$	-	177	270	m $\Omega$
	N		$V_{GS}=4.5\text{ V}, I_D=-1.1\text{ A}$	-	191	280	
	P		$V_{GS}=-10\text{ V}, I_D=-1.5\text{ A}$	-	113	150	
	N		$V_{GS}=10\text{ V}, I_D=1.4\text{ A}$	-	119	160	
Transconductance	P	$g_{fs}$	$ V_{DS} >2 I_D R_{DS(on)max}, I_D=-1.18\text{ A}$	-	2.7	-	S
	N		$ V_{DS} >2 I_D R_{DS(on)max}, I_D=1.1\text{ A}$	-	2.3	-	

<sup>2)</sup> Performed on 40mm<sup>2</sup> FR4 PCB. The traces are 1mm wide, 70 $\mu\text{m}$  thick and 20mm long; they are present on both sides of the PCB

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

**Dynamic characteristics**

Input capacitance	P	$C_{iss}$	$V_{GS}=0\text{ V}$ , P: $V_{DS}=-15\text{ V}$ , N: $V_{DS}=15\text{ V}$ , $f=1\text{ MHz}$	-	212	282	pF			
	N			-	71	94				
Output capacitance	P	$C_{oss}$		$V_{GS}=0\text{ V}$ , P: $V_{DS}=-15\text{ V}$ , N: $V_{DS}=15\text{ V}$ , $f=1\text{ MHz}$	-	69	91	pF		
	N				-	26	35			
Reverse transfer capacitance	P	$C_{rss}$			$V_{GS}=0\text{ V}$ , P: $V_{DS}=-15\text{ V}$ , N: $V_{DS}=15\text{ V}$ , $f=1\text{ MHz}$	-	56	84	pF	
	N					-	5	7		
Turn-on delay time	P	$t_{d(on)}$				P: $V_{DD}=-15\text{ V}$ , $V_{GS}=-10\text{ V}$ , $R_G=6\ \Omega$ , $I_D=-1.5\text{ A}$	-	5.0	-	ns
	N						-	3.4	-	
Rise time	P	$t_r$	P: $V_{DD}=-15\text{ V}$ , $V_{GS}=-10\text{ V}$ , $R_G=6\ \Omega$ , $I_D=-1.5\text{ A}$				-	6.5	-	ns
	N						-	2.3	-	
Turn-off delay time	P	$t_{d(off)}$		N: $V_{DD}=15\text{ V}$ , $V_{GS}=10\text{ V}$ , $R_G=6\ \Omega$ , $I_D=1.4\text{ A}$			-	14.3	-	ns
	N						-	5.8	-	
Fall time	P	$t_f$			N: $V_{DD}=15\text{ V}$ , $V_{GS}=10\text{ V}$ , $R_G=6\ \Omega$ , $I_D=1.4\text{ A}$		-	7.5	-	ns
	N						-	1.0	-	

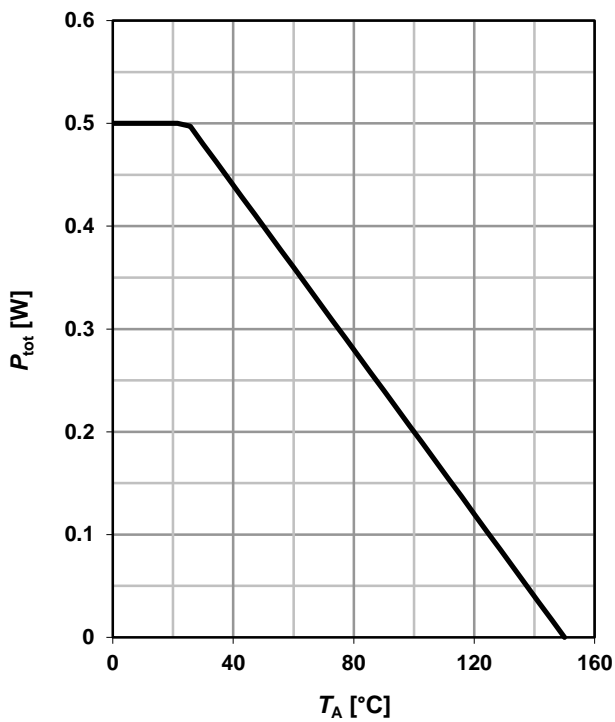
**Gate Charge Characteristics**

Gate to source charge	P	$Q_{gs}$	$V_{DD}=-15\text{ V}$ , $I_D=-1.5\text{ A}$ , $V_{GS}=0\text{ to }-5\text{ V}$	-	-0.6	-	nC
Gate to drain charge		$Q_{gd}$		-	-1.2	-	
Switching charge		$Q_g$		-	-2.4	-	
Gate plateau voltage		$V_{plateau}$		-	-2.9	-	
Gate to source charge	N	$Q_{gs}$	$V_{DD}=15\text{ V}$ , $I_D=1.4\text{ A}$ , $V_{GS}=0\text{ to }5\text{ V}$	-	0.3	-	nC
Gate to drain charge		$Q_{gd}$		-	0.2	-	
Switching charge		$Q_g$		-	0.6	-	
Gate plateau voltage		$V_{plateau}$		-	3.4	-	

Parameter	Symbol	Conditions	Values			Unit	
			min.	typ.	max.		
<b>Reverse Diode</b>							
Diode continuous forward current	P	$I_S$	$T_C=25\text{ °C}$	-	-	-0.5	A
	N			-	-	0.5	
Diode pulse current	P	$I_{S,pulse}$		-	-	-6.0	
	N			-	-	5.6	
Diode forward voltage	P	$V_{SD}$	$V_{GS}=0\text{ V}, I_F=-1.5\text{ A}, T_j=25\text{ °C}$	-	-0.8	-1.1	V
	N			$V_{GS}=0\text{ V}, I_F=1.4\text{ A}, T_j=25\text{ °C}$	-	0.86	
Reverse recovery time	P	$t_{rr}$	$V_R=\pm 15\text{ V}, I_F=I_S, di_F/dt=100\text{ A}/\mu\text{s}$	-	8.2	-	ns
	N			-	9.1	-	
Reverse recovery charge	P	$Q_{rr}$		-	2.1	-	nC
	N			-	2.6	-	

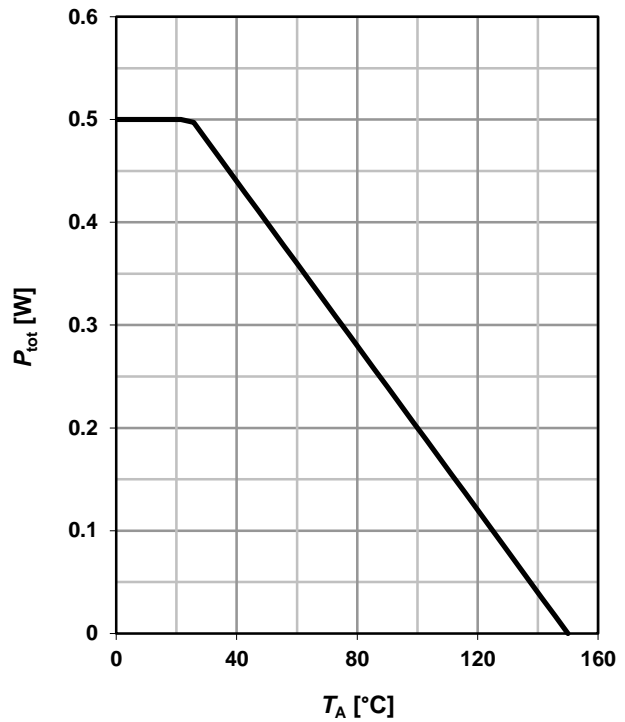
**1 Power dissipation (P)**

$P_{tot}=f(T_A)$



**2 Power dissipation (N)**

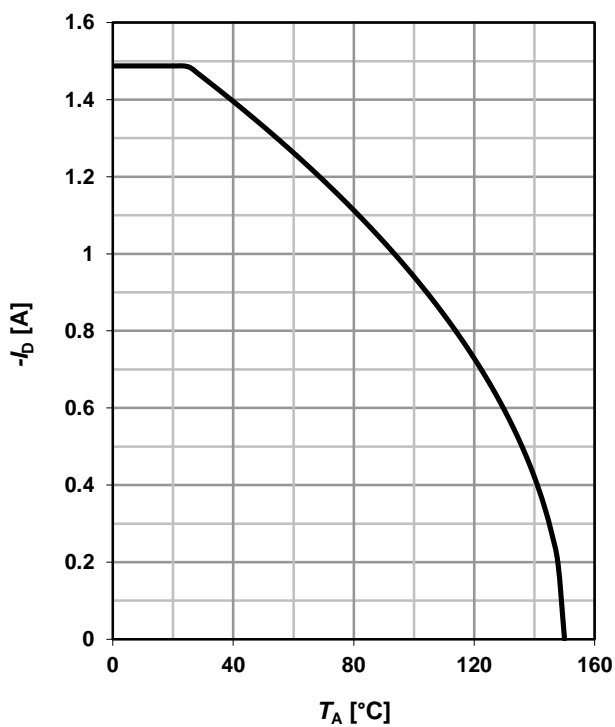
$P_{tot}=f(T_A)$



**3 Drain current (P)**

$I_D=f(T_A)$

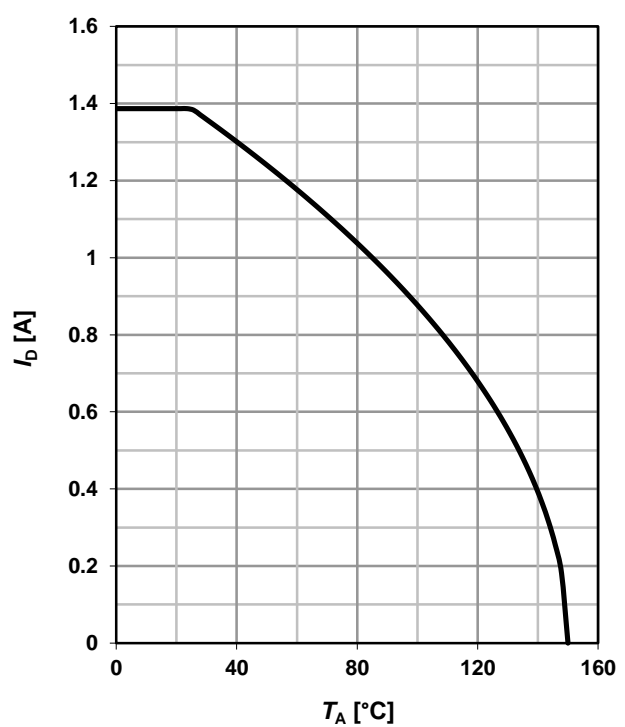
parameter:  $V_{GS} \leq -10$  V



**4 Drain current (N)**

$I_D=f(T_A)$

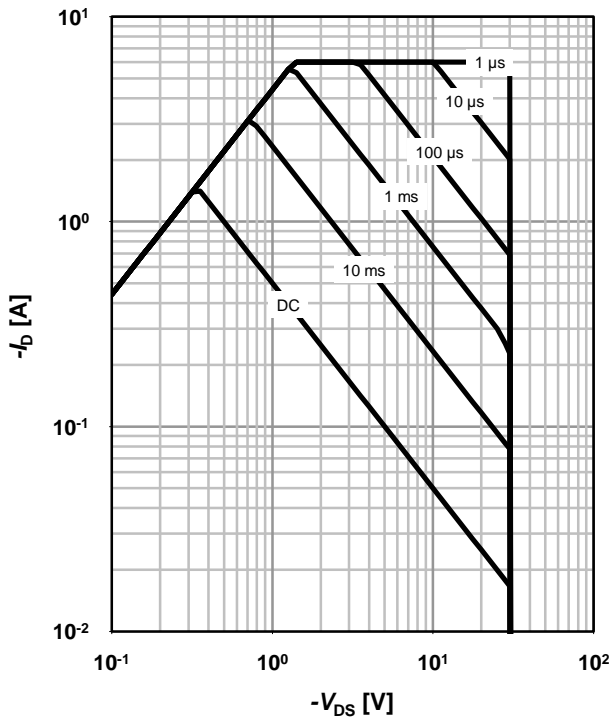
parameter:  $V_{GS} \geq 10$  V



**5 Safe operating area (P)**

$I_D=f(V_{DS}); T_A=25\text{ }^\circ\text{C}; D=0$

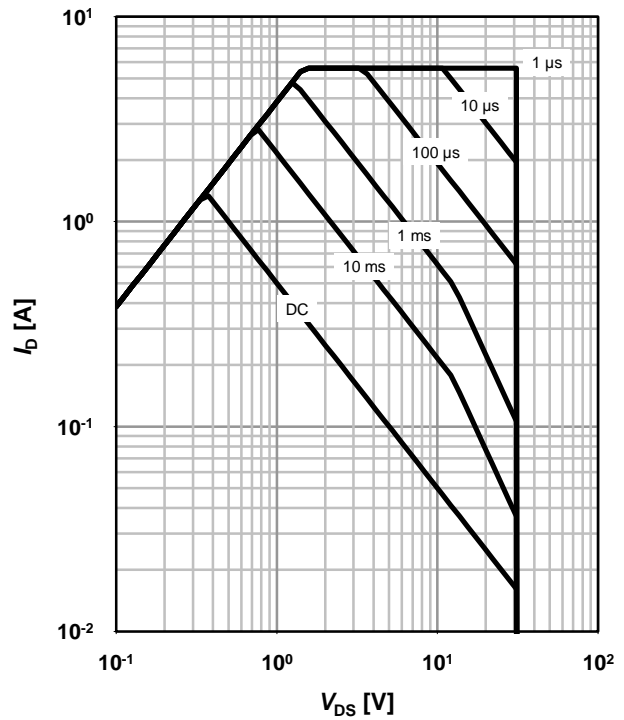
parameter:  $t_p$



**6 Safe operating area (N)**

$I_D=f(V_{DS}); T_A=25\text{ }^\circ\text{C}; D=0$

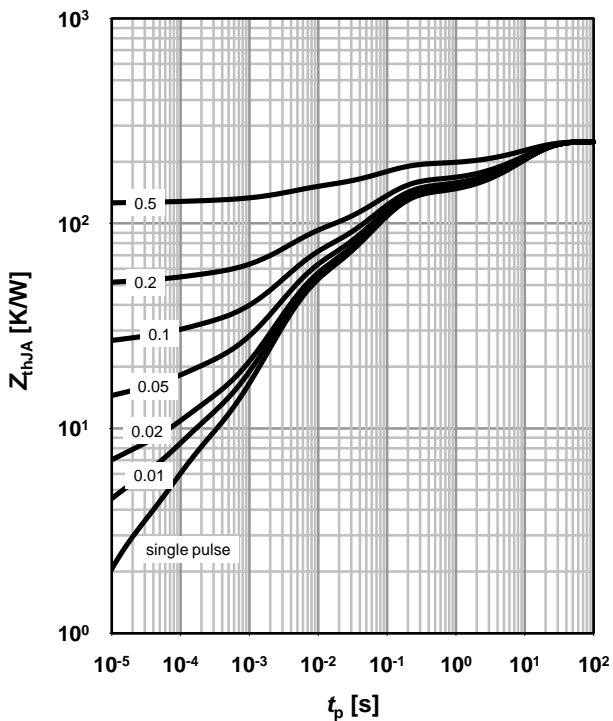
parameter:  $t_p$



**7 Max. transient thermal impedance (P)**

$Z_{thJA}=f(t_p)$

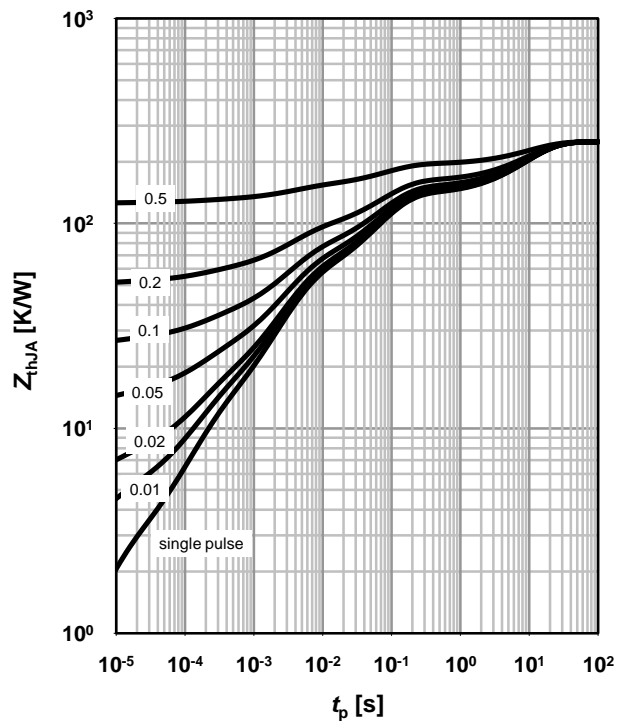
parameter:  $D=t_p/T$



**8 Max. transient thermal impedance (N)**

$Z_{thJA}=f(t_p)$

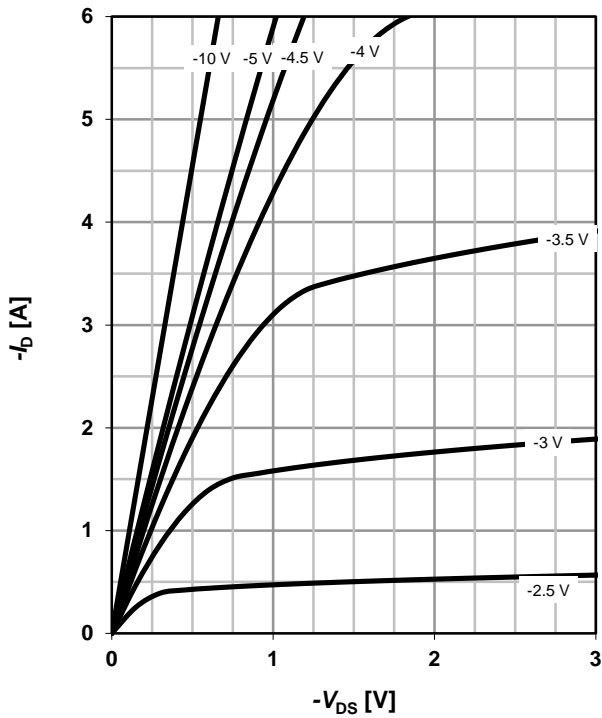
parameter:  $D=t_p/T$



**9 Typ. output characteristics (P)**

$I_D=f(V_{DS}); T_j=25\text{ }^\circ\text{C}$

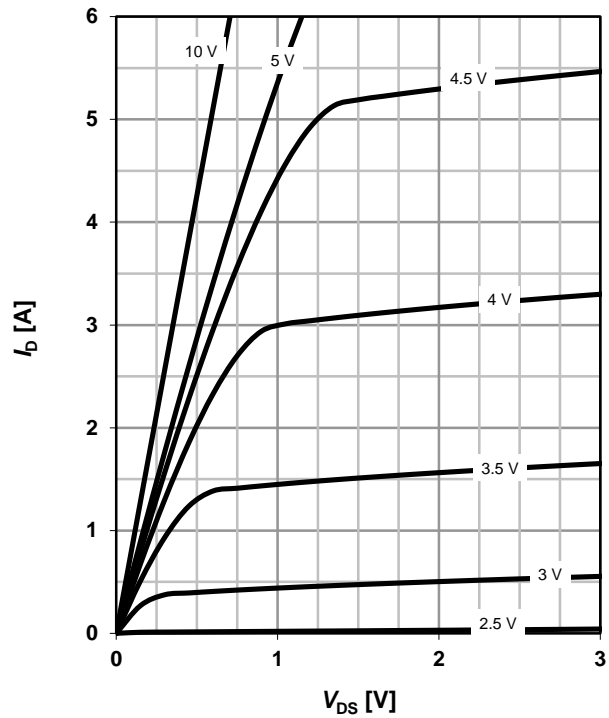
parameter:  $V_{GS}$



**10 Typ. output characteristics (N)**

$I_D=f(V_{DS}); T_j=25\text{ }^\circ\text{C}$

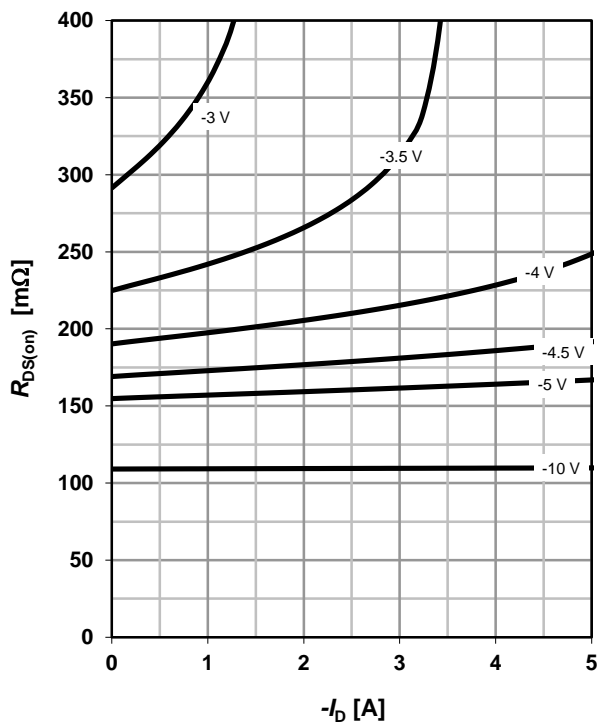
parameter:  $V_{GS}$



**11 Typ. drain-source on resistance (P)**

$R_{DS(on)}=f(I_D); T_j=25\text{ }^\circ\text{C}$

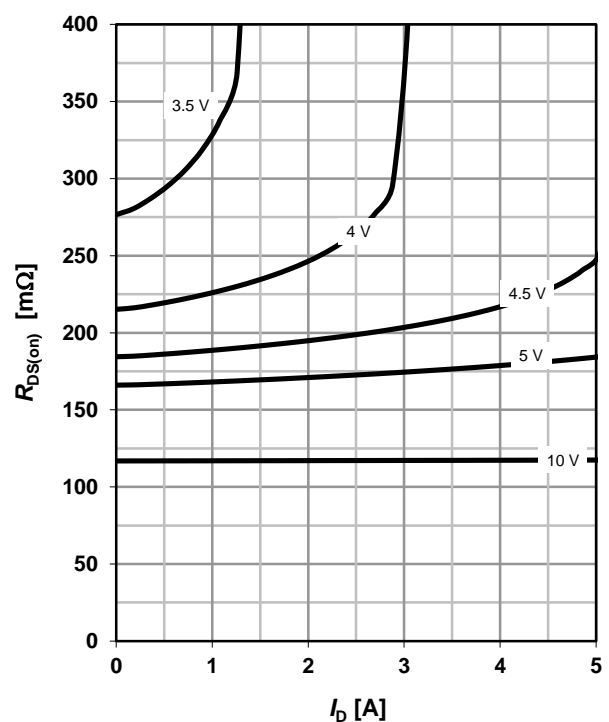
parameter:  $V_{GS}$



**12 Typ. drain-source on resistance (N)**

$R_{DS(on)}=f(I_D); T_j=25\text{ }^\circ\text{C}$

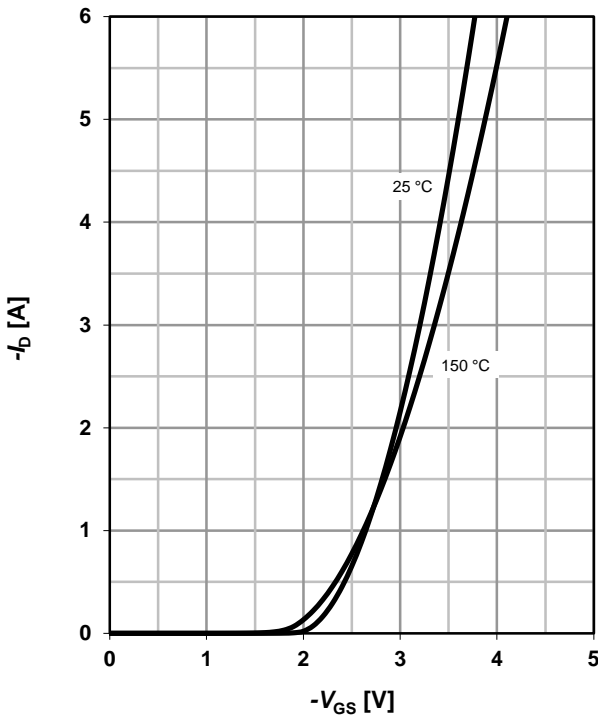
parameter:  $V_{GS}$



**13 Typ. transfer characteristics (P)**

$$I_D = f(V_{GS}); |V_{DS}| > 2 |I_D| R_{DS(on)max}$$

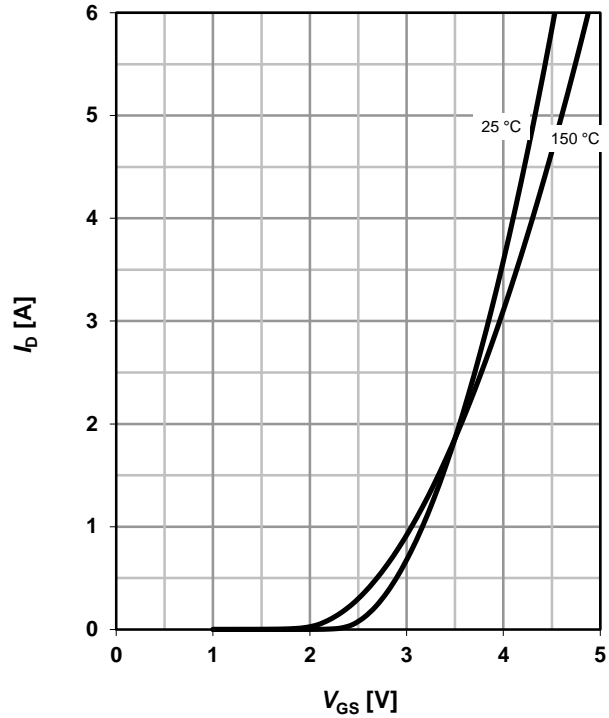
parameter:  $T_j$



**14 Typ. transfer characteristics (N)**

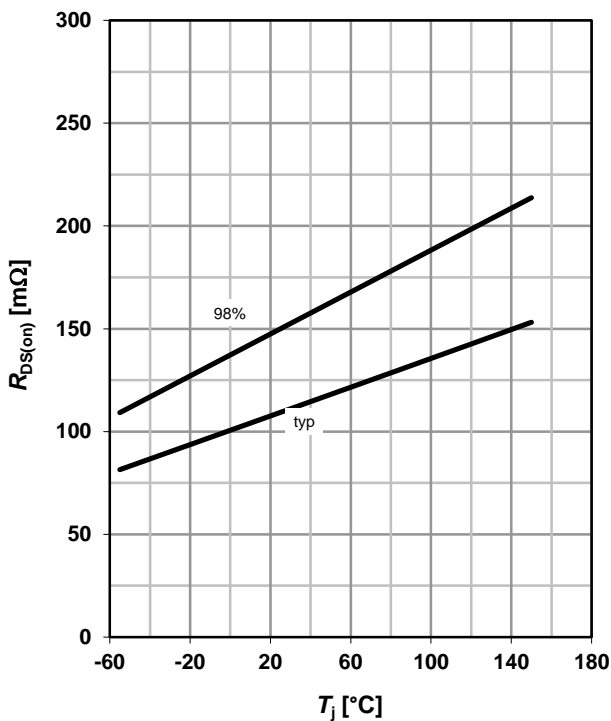
$$I_D = f(V_{GS}); |V_{DS}| > 2 |I_D| R_{DS(on)max}$$

parameter:  $T_j$



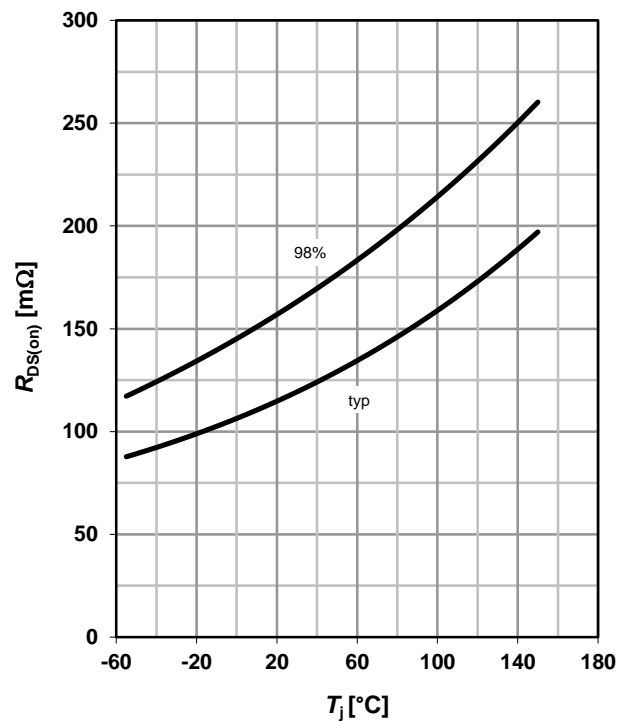
**15 Drain-source on-state resistance (P)**

$$R_{DS(on)} = f(T_j); I_D = -1.5 \text{ A}; V_{GS} = -10 \text{ V}$$



**16 Drain-source on-state resistance (N)**

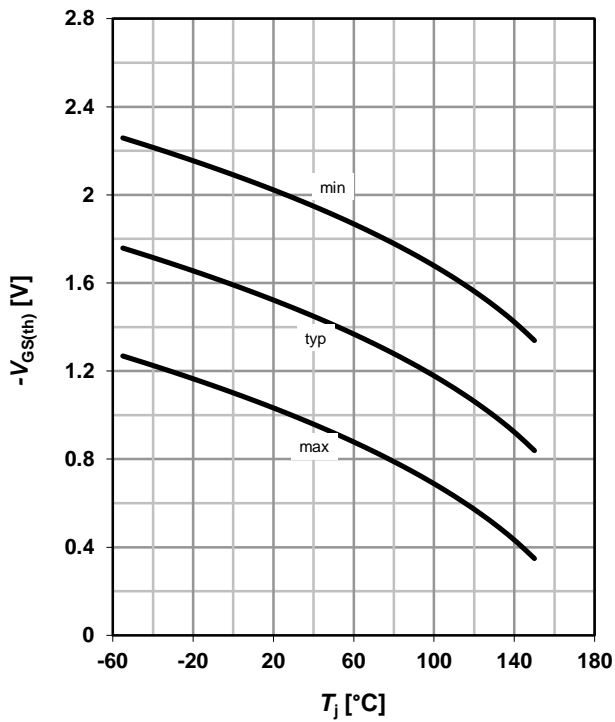
$$R_{DS(on)} = f(T_j); I_D = 1.4 \text{ A}; V_{GS} = 10 \text{ V}$$





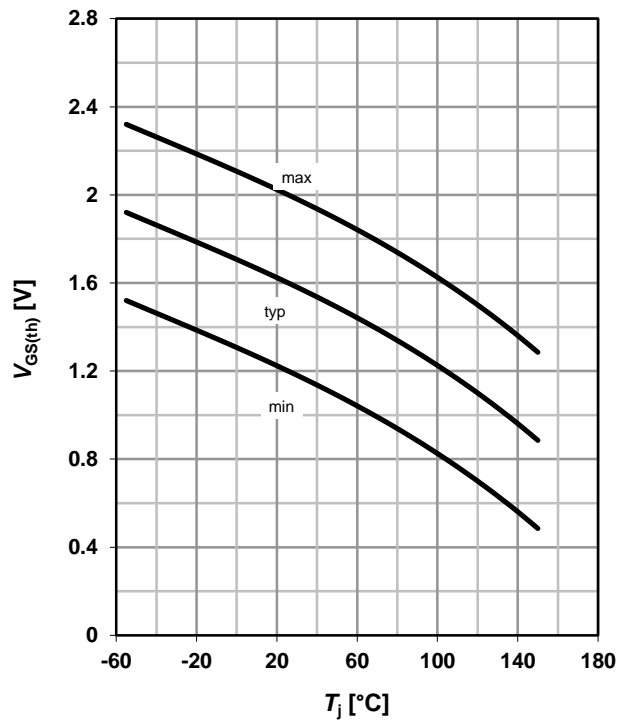
**17 Typ. gate threshold voltage (P)**

$V_{GS(th)}=f(T_j)$ ;  $V_{GS}=V_{DS}$ ;  $I_D=-11 \mu A$



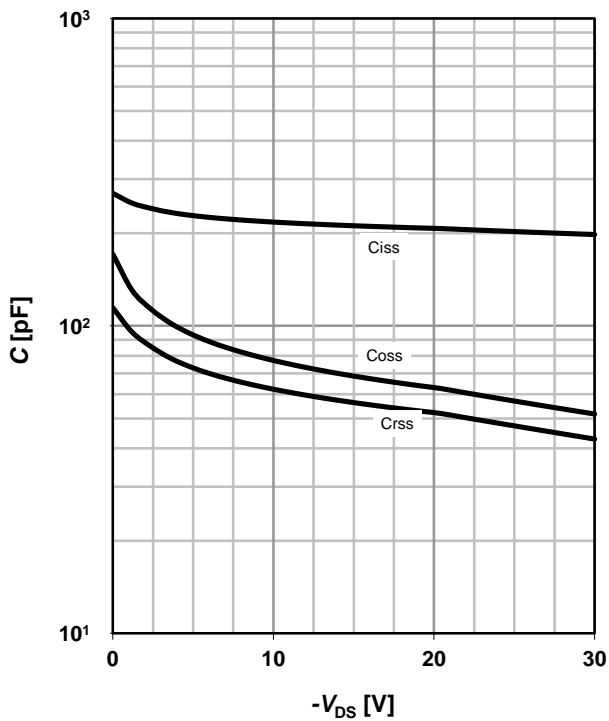
**18 Typ. gate threshold voltage (N)**

$V_{GS(th)}=f(T_j)$ ;  $V_{GS}=V_{DS}$ ;  $I_D=3.7 \mu A$



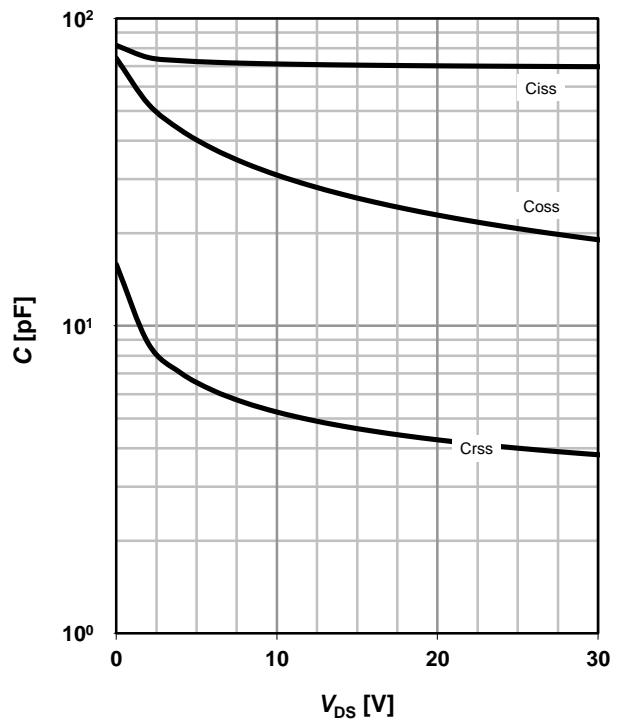
**19 Typ. capacitances (P)**

$C=f(V_{DS})$ ;  $V_{GS}=0 V$ ;  $f=1 MHz$



**20 Typ. capacitances (N)**

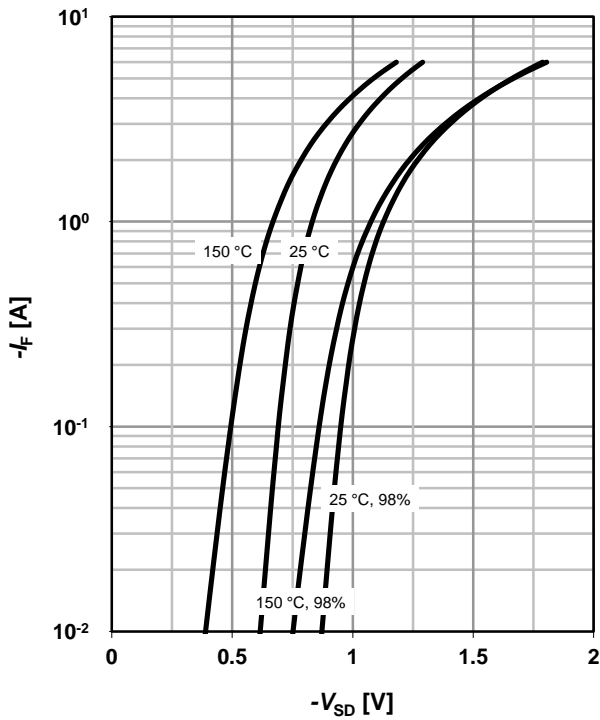
$C=f(V_{DS})$ ;  $V_{GS}=0 V$ ;  $f=1 MHz$



**21 Forward characteristics of reverse diode (P)**

$I_F=f(V_{SD})$

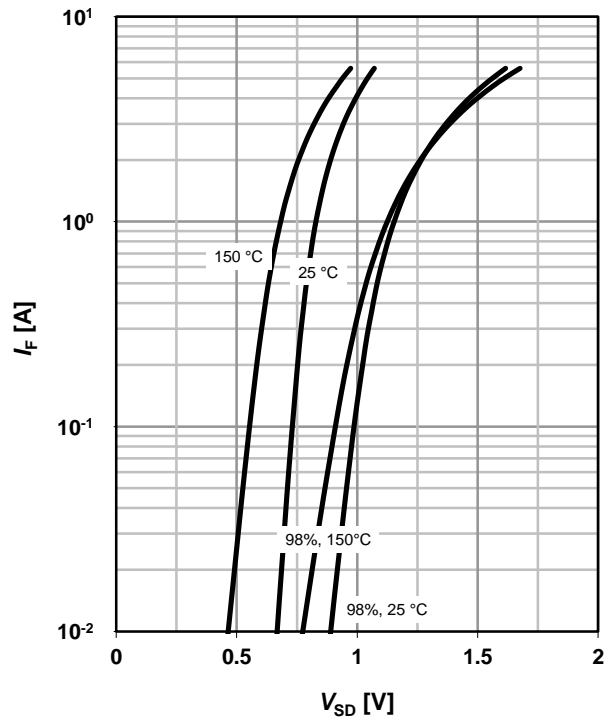
parameter:  $T_j$



**22 Forward characteristics of reverse diode (N)**

$I_F=f(V_{SD})$

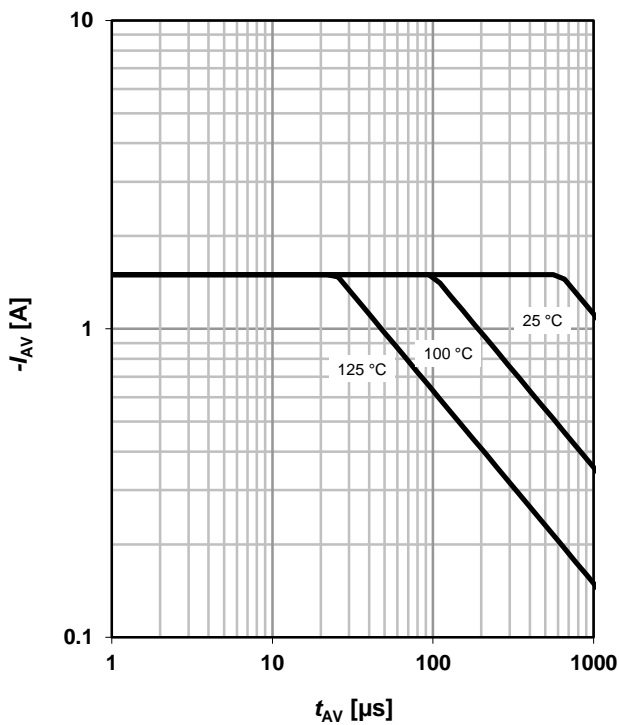
parameter:  $T_j$



**23 Avalanche characteristics (P)**

$I_{AS}=f(t_{AV}); R_{GS}=25 \Omega$

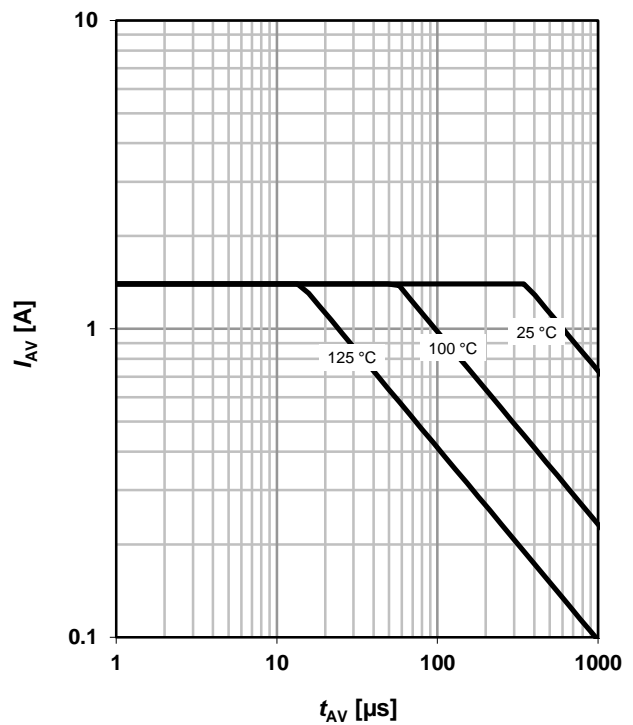
parameter:  $T_{j(start)}$



**24 Avalanche characteristics (N)**

$I_{AS}=f(t_{AV}); R_{GS}=25 \Omega$

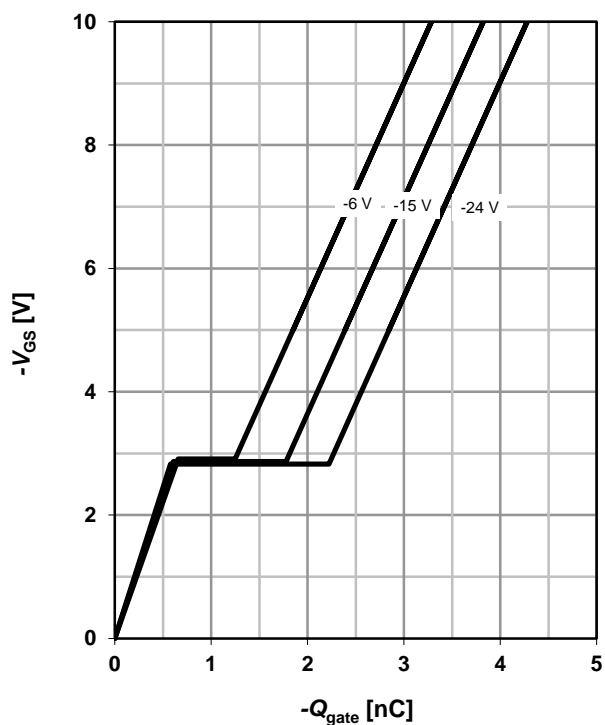
parameter:  $T_{j(start)}$



**25 Typ. gate charge (P)**

$V_{GS}=f(Q_{gate}); I_D=-1.5$  A pulsed

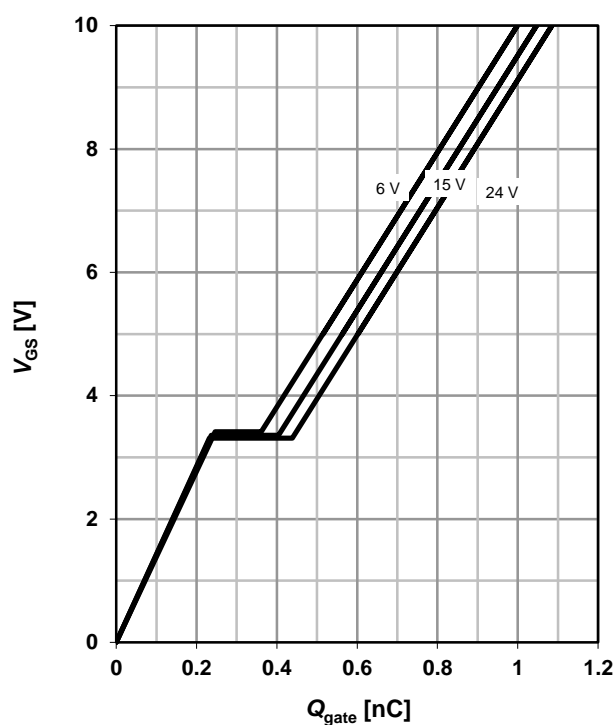
parameter:  $V_{DD}$



**26 Typ. gate charge (N)**

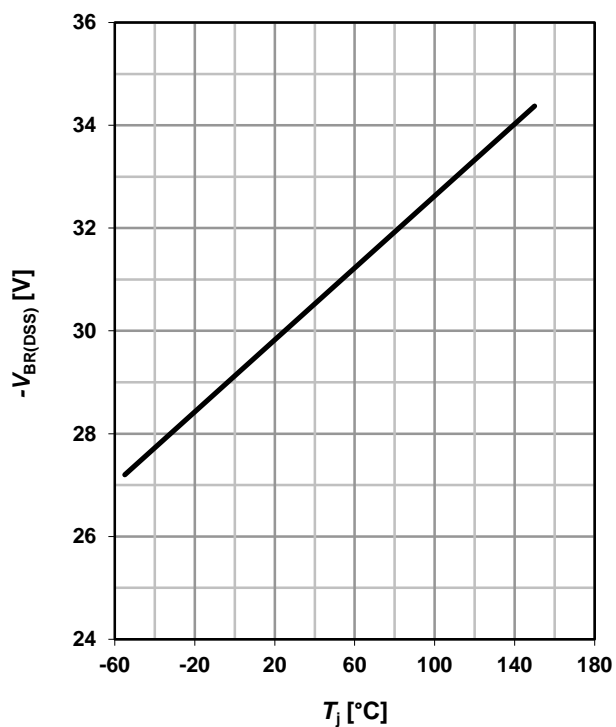
$V_{GS}=f(Q_{gate}); I_D=1.4$  A pulsed

parameter:  $V_{DD}$



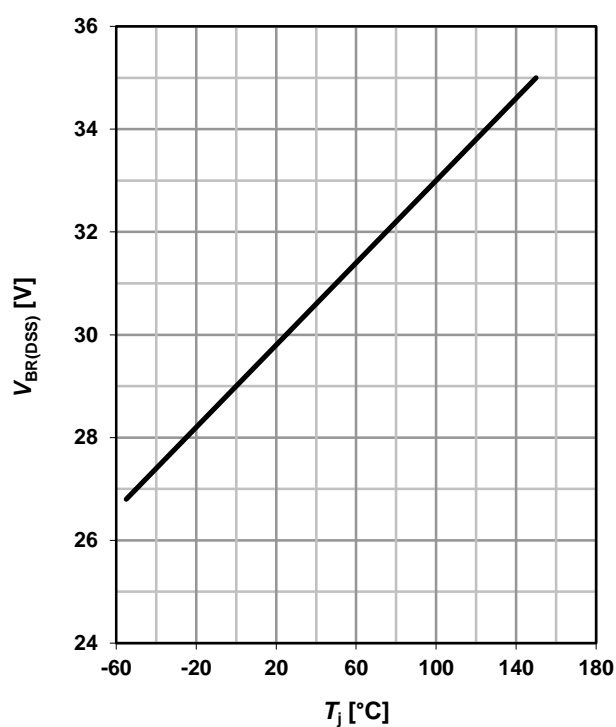
**27 Drain-source breakdown voltage (P)**

$V_{BR(DSS)}=f(T_j); I_D=-250$   $\mu$ A



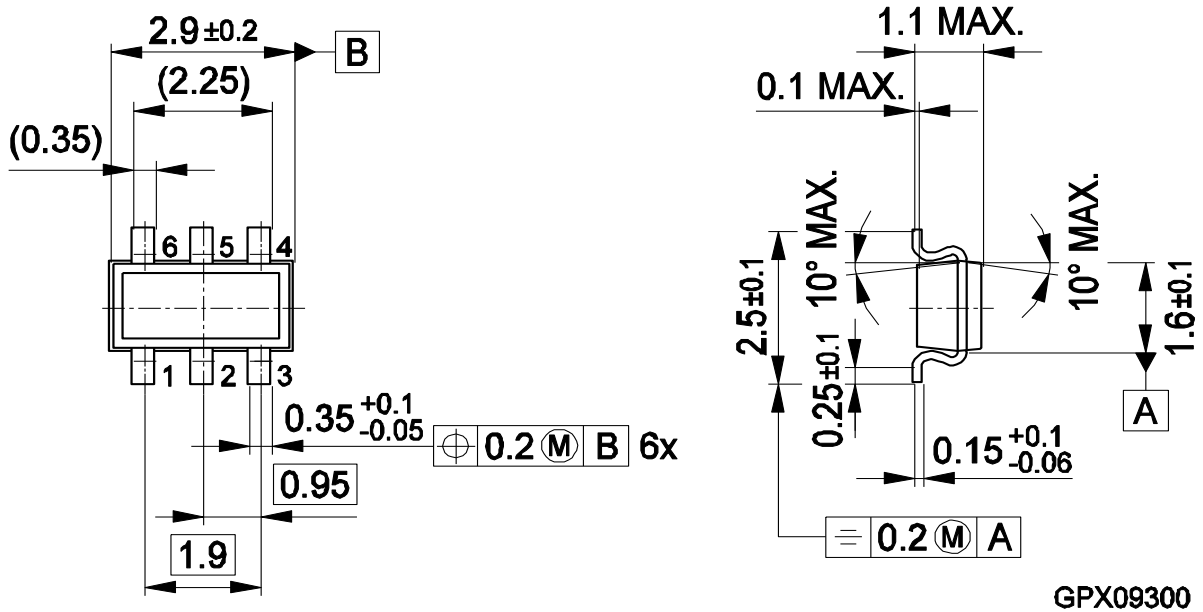
**28 Drain-source breakdown voltage (N)**

$V_{BR(DSS)}=f(T_j); I_D=250$   $\mu$ A



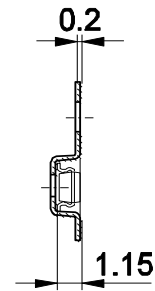
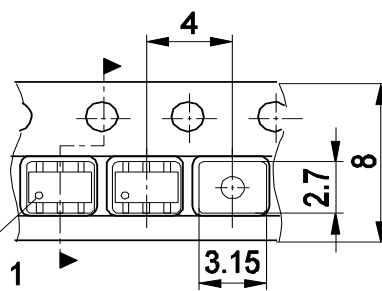
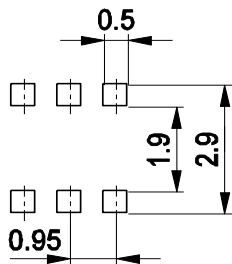
Package Outline:

TSOP6



Footprint:

Packaging:



Remark: Wave soldering possible dep. on customers process conditions.  
Pin 1 marking

HLG09283

CPWG5899

Dimensions in mm

Note: For symmetric types there is no defined Pin 1 orientation in the reel.

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